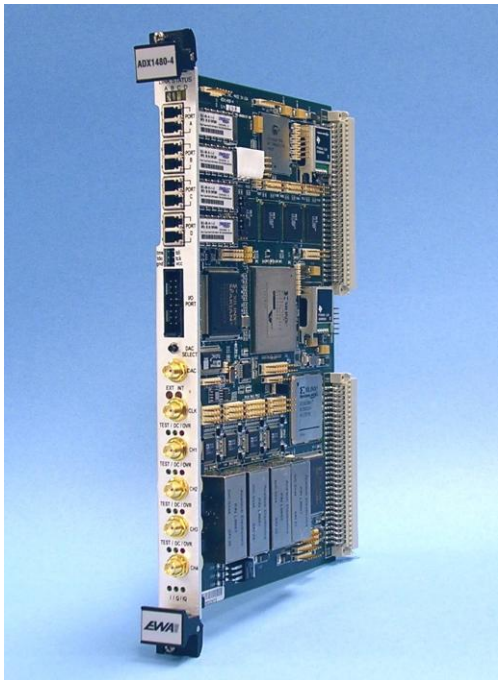
EWA Government Systems, Inc.
"Enabling a more secure future"

ADX1480-4 High Performance A/D Module



Features

- 4 -80MSPS, 14-bit, ADC's
- 2M – 6M Gate Virtex II Front End Processing FPGA
- 4 -1Gbps FibreXtreme Compliant FO Ports capable of 100 MB/s sustained transmit rates
- 4 -1MB x 9 Transmit FIFOs
- Electronically selectable sample clock source
- Front panel selectable analog test output port
- Electronically selectable AC or DC coupling, or 50Ω input termination on each analog input channel
- User definable real-time control from front panel or VME P2 interface.
- Optional anti-aliasing input filters

General Description

EWA's ADX1480-4 is a 4-channel, 80MSPS ADC module with highly configurable front end processing capabilities. This module contains four identical input channels, each sampled by an electronically selected internal or external clock source. Each channel has provisions for an anti-alias filter and can be independently configured as AC or DC coupled. Front End Processing is performed in a high speed, high capacity Xilinx Virtex-II FPGA. Processed data is output through any combination of 4 fully independent, FibreXtreme compliant, 1 Gbps Fiber Optic ports.

Board Specifications

Input Clock Frequency:	30 to 80 MHz
Input Clock Power Level:	-10 to +10dB (sine or square wave)
Channel Input Levels:	+12dBm max (overdrive indicator LED for each channel)
Ch - Ch Isolation:	65dB min
Open circuit isolation:	34dB typ
DAC Output power:	-4dBm max
DAC output frequency:	125MHz max
Fiber Output frequency:	850 nm, multimode (1310 nm optional)
Power requirements:	4A @ +5VDC; 168mA @ -12VDC

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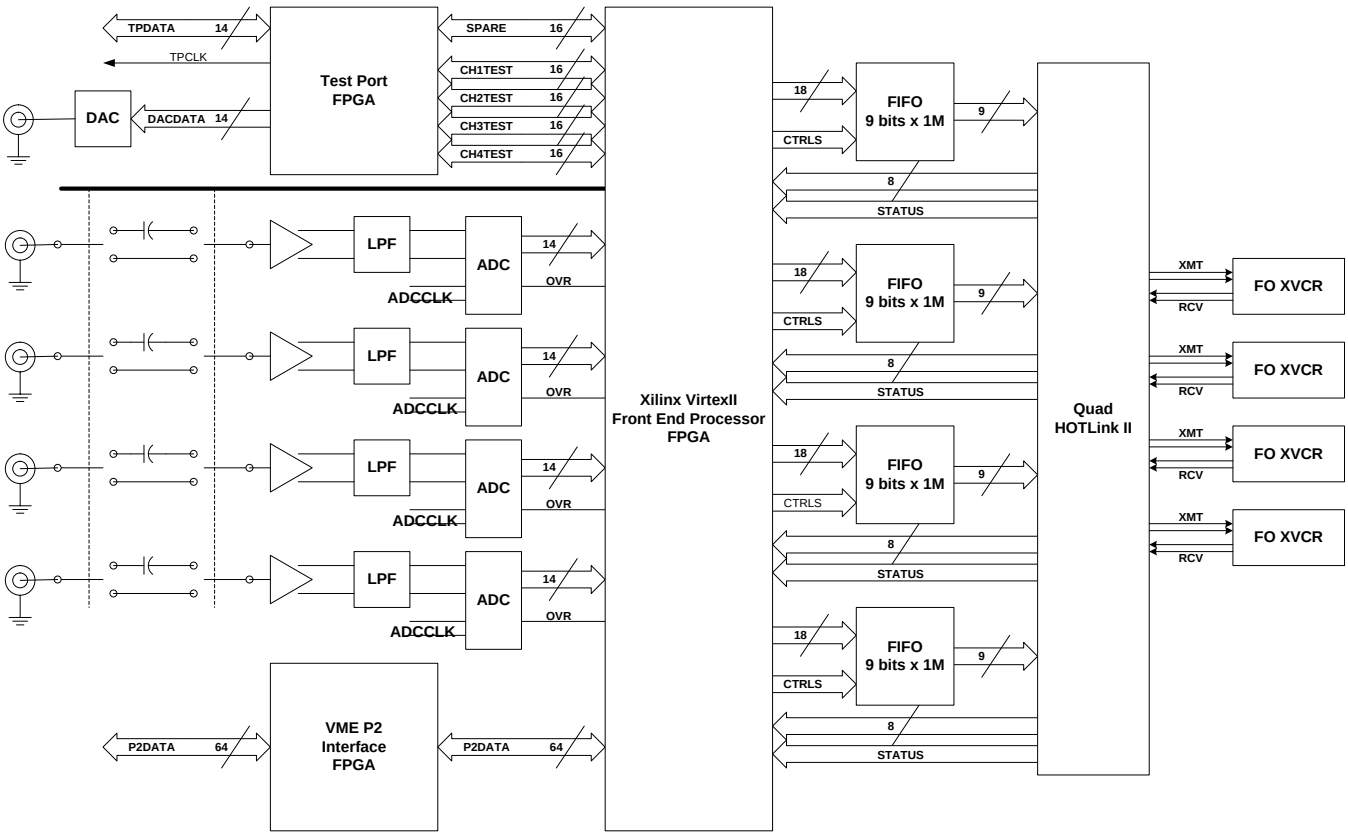
Block Diagram



Applications

Digital Receiver

The ADX1480-4 has been used as a digital IF receiver for several radar systems. For this purpose, the on-board Xilinx Virtex-II FPGA has been programmed to perform digital I/Q demodulation followed by selectable filter/decimate stages. Sets of user specified filter characteristics are downloaded to the board on initialization, and selections of specific filters are made in real-time. As many as 24 simultaneous range-gated channels have been implemented, each with its own filter/decimate chain.

Coherent Sidelobe Canceller (SLC)

An SLC module was implemented on the ADX1480-4 for a radar system using two auxiliary receiver antennas to cancel jamming signals received by the main radar antenna from two separate locations. The canceller implementation required precise time alignment in various computation paths within the firmware. Following the cancellation functions, the digital radar signal is converted back to an analog IF output using the on-board DAC.

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