EWA Government Systems, Inc.
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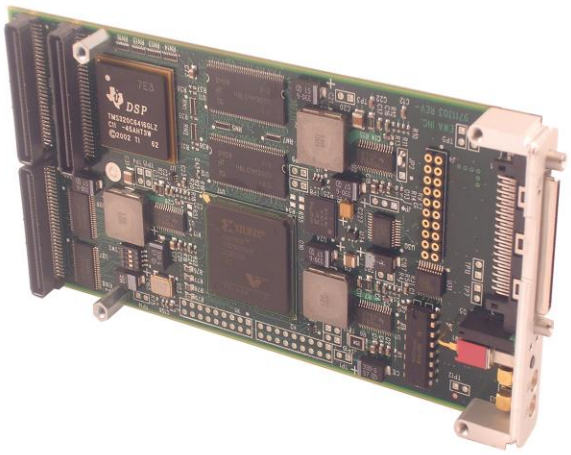
PMC TCU Timing and Control Unit



Features

- Single Universal 32 bit, 33 MHz PMC Module, Slot 0 Controller Capability
- Provides Real-time Scheduling with Resolution down to 20 ns (50 MHz System Clock)
- Up to 64 Events Scheduled per System Clock Cycle
- User Defined Application runs on Texas Instruments TMS320C6416 DSP
- Xilinx FPGA used for Application Specific I/O Logic
- 64 5V Tolerant LVTTL I/O's via PMC P14 User I/O Connector
- 32 Differential LVDS Outputs on Front Panel, up to 8 can be Configured as Inputs
- JTAG Port for DSP and FPGA Programming

General Description

The PMC Timing and Control Unit (TCU) is a single slot PCI Mezzanine Card (PMC) that schedules real time events with resolutions as fine as 20 nanoseconds. Using this board, a designer can develop applications that schedule real-time signals with fine resolution and precision under software control.

The key elements of the TCU's architecture are a Texas Instruments TMS320C6416 (C6416) processor running application-specific software, 1 MB of L2 cache within the C6416 configured as a ring buffer of 64 bit wide memory called the Time Slice RAM (TSR), and a Xilinx FPGA.

Timing is based on the system clock which can be either an on-board oscillator or an external clock. In either case, the maximum clock frequency is 50 MHz when using 32 bit TSR and 44 MHz when using 64 bit TSR.

The software application running on the C6416 writes to the TSR to schedule individual bits. The TSR is a 32 or 64 bit wide ring buffer where each address represents a "slice in time." The FPGA sequentially reads through the TSR at the system clock rate. This allows for the continuous cycling of scheduled data. The C6416 can schedule events to happen in the very near future by writing to an address just a few ticks ahead of the current address pointer. It can also schedule events further into the future by writing to addresses many ticks ahead of the current address pointer.

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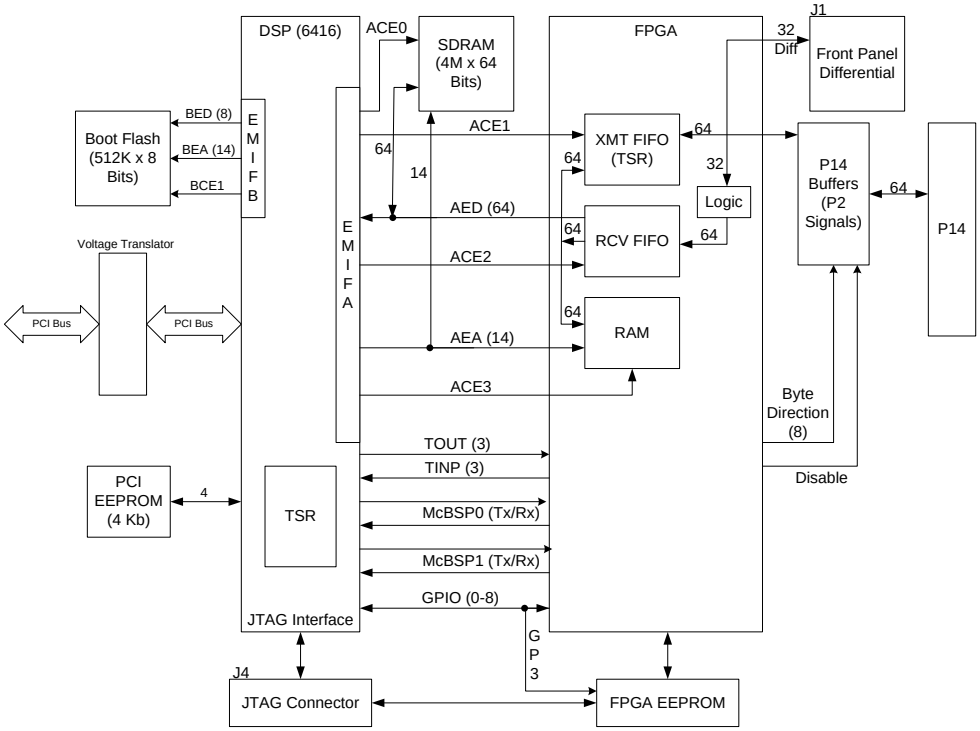
General Description (continued)

The FPGA contains the TSR FIFO and I/O logic. On each edge of the system clock, 32 bits of data are output from the TSR FIFO in 32 bit TSR mode and 64 bits are output in 64 bit TSR mode. These bits can be manipulated in the FPGA to produce skews, delays, combinational logic outputs, serial messages, clocks or any other logic function desired. The manipulated bits can then be output via the P14 and/or front panel connectors for up to 64 LVTTL plus 32 LVDS outputs. Data can also come into the FPGA via these connectors. Up to 8 inputs are allowed on the front panel connector and 64 inputs are allowed on the P14 connector. Typically status will come into the FPGA from other boards in the system and this status can be passed to the C6416. Multiple TCU's can be synchronized to each other to increase both the number of system real-time I/O's and available scheduling power.

Typical applications of the PMC TCU are real-time control for systems and test environments including radar and sonar and other applications requiring deterministic hardware control.

Block Diagram



Available VME Accessories

TTL Companion Board - Single-slot 6U VME module provides 64 differential outputs and 3 open emitter outputs from VME P2.

Fiber Optic Companion Board – Single-slot 6U VME module provides 6 Fibre Channel I/Os from VME P2 for long distance control.

P2 Paddle Card - provides 25 differential outputs from VME P2 rear.

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